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METHODS AND CIRCUITRY FOR IMPLEMENTING FIRST-IN FIRST-OUT STRUCTURE

CROSS-REFERENCE TO RELATED APPLICATION(S)

This application is a divisional of Application No. 09/956,374, filed September 17, 2001, which is now a U.S. Patent 6,696,854 the disclosure of which is incorporated herein by reference.[1]

FIELD OF THE INVENTION

The present invention relates in general to integrated circuits, and in particular to method and circuitry for implementing high speed first-in-first-out (FIFO) structures.

BACKGROUND

FIFOs are used in a variety of circuit applications. For example, data communication circuits use FIFO structures to address different system timing requirements. A serializer, for example, employs an internal clock that may not be synchronized with an external clock used to supply data to the circuit. A FIFO is used to transfer the data from the external clock regime to the internal clock regime. Typically, such a FIFO includes a number of registers that operate in response to a write pointer and a read pointer. An external clock usually provides or controls the write pointer while an internal clock controls the read pointer. Even though the phase relationship between these two clock domains is arbitrary, conventional FIFO designs require the frequencies of the two clock signals to be the same. There are applications, however, that require one clock domain to be of different frequency compared to the other (e.g., the write clock frequency be half that of the read clock, or vice versa). Furthermore, FIFOs require additional control

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